24-12-2019

Indira Gandhi Delhi Technical University for Women

(Established by Govt. of Delhi vide Act 09 of 2012)

Kashmere Gate, Delhi - 110006

JCT based One Week STC on "Design Challenges in Low Power VLSI Design"

Department of Electronics & Communication Engineering (ECE), IGDTUW, Kashmere Gate organized one week lCT based Short Term Programme on "Design Challenges in Low Power VLSI Design" in collaboration with NITTTR Chandigarh during 16th - 20th December, 2019. The venue of the Programme was DSP Lab, Room No. I09, EC E Department. Course Content covered in one wee k ICT based Short Term Programme Challenges in low Power Design, IC Fabrication, Evolutionary Approach to VLSI CAD, Concepts of Low Power Design, Concepts of Low Power Des ig n, VHDL Programming, Nano Scale Semi-Conductor Dev ices, Low Power Memory Design, Cogenda T-CAD, Cogenda T-CA D, Cogenda T-CAD, Advances in materials for VLSI Application, VLSI Devices for Low Power Applications. Th e program was exceptionally beneficial for the faculty members of ECE\department. The FOP was attended by nearly 48 participants including faculties, lab ass is tants.30 M tech students and 28 rese arch scholars.

Co-ordinator

Dr Richa Yadav
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